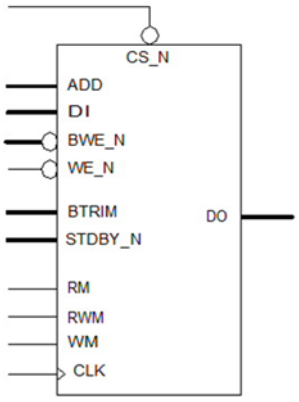
RF1P-HS-TS22ULL

Single Port

Register File Compiler



Ultra-Low Leakage: High V_T (HV_T) are used to minimize leakage performance.

Bit Cell: Utilizes Foundry's 6T bit cells to ensure high manufacturing yields

Deep Sleep Mode Retains data a minimal power consumption. Dedicated standby mode reduces power required to an absolute minimum to retain the memory contents.

Isolated Array and Periphery supplies: Periphery voltage can be shut off to further reduce standby power. Both periphery and array can be supplied with the same .9 V Supply

Adjustable Internal Read and Write Timing Margins

BIST Muxes can optionally be added to the wrapper

Bit Write Enable: Allows independent write operations to any subset of a memory word.

Technology	22ULL
Voltage	0.9V (0.81V to 0.99V)
Temperature	-40°C to +125°C
Power	Mesh
# Metal Layers	4
BIST Mux	Internal
Modes	Functional, BIST, Scan, Sleep

Max Instance	78K bits
Min Instance	128 Bits
Word Width	8 – 148
Word Depth	8-1024
Aspect Ratio	Column Fold: 2 or 4
User Interface	Command Line
Bit Write Enable	Optional

EDA Views (Partial List)	
Verilog Model with UPF	
Liberty Files (NLDM, LVF, CCS)	
PDF and Text Datasheets	Redhawk APL
LEF 5.8	Verilog Test Bench
LVS SPICE Netlist	Bitmap File (x, y)
GDS	Power Grid (Voltus)
Tessent MBIST Control File	Common Power Format (CPF)

About Mobile Semiconductor:

Nordic Semiconductor's Seattle, Washington memory team continues building on the technology acquired from Mobile Semiconductor. SRAM, ROM, and Register File compilers are available for applications requiring ultra-low power, low leakage, or ultra-high performance.

http://www.mobile-semiconductor.com/