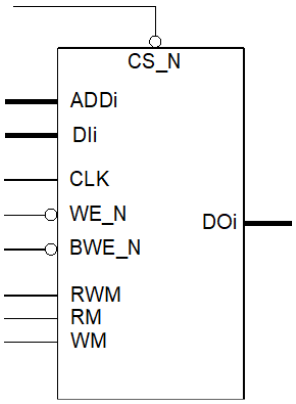
Single Port High Speed

SP-HS-TS22ULL

SRAM Memory Compiler

22ULL Process



High Performance: Array is split into multiple banks to reduce the length of each bit line improve timing.

Ultra-Low Leakage: High V_T (HV_T) devices are used with source biasing to minimize leakage currents.

Bit Cell: Utilizes Premier Fab's Low Leakage 6T bit cells to ensure high manufacturing yields

Ultra Low Power Standby: Dedicated Standby mode with optional built in source biasing.

Isolated Array and Periphery supplies: Periphery voltage can be shut off to further reduce standby power

Data Write-Through: Pin controllable write through disables data out transitions during a write to reduce power. During ATPG data out is controllable to ensure full coverage

Error Correction: Single bit error correction and dual bit error detection (SECDED) is optionally included in the synthesizable wrapper.

Technology	22ULL
Voltage	0.9V (0.81V to 0.99V)
Temperature	-40°C to +125°C
Power	Mesh
# Metal Layers	4
BIST Mux	Internal
Modes	Functional, BIST, Sleep

Max Instance	288Kbits
Min Instance	256 Bits
Word Width	8 –144
Word Depth	32 – 4096
Aspect Ratio	Column Fold: 4 or 8
Write Through	Pin control
Bit Write Enable	Optional
User Interface	Command Line

EDA Views (Partial List)	
Verilog Model with UPF	
Liberty Files (NLDM, LVF, CCS)	
PDF and Text Datasheets	Redhawk APL
LEF 5.8	Verilog Test Bench
LVS SPICE Netlist	Bitmap File (x, y)
GDS	Power Grid (Voltus)
Tessent MBIST Control File	Common Power Format (CPF)

About Mobile Semiconductor:

Nordic Semiconductor's Seattle, Washington memory team continues building on the technology acquired from Mobile Semiconductor. SRAM, ROM, and Register File compilers are available for applications requiring ultra-low power, low leakage, or ultra-high performance.

http://www.mobile-semiconductor.com/