SP-ULL-GF22FDX

Single Port Low Leakage

SRAM Memory Compiler

Ultra-Low Leakage: High V_T (HV_T) and low leakage ($LLHV_T$) devices are used with source biasing to minimize standby currents while operating at low voltage

Bit Cell: Utilizes GlobalFoundries® Ultra-Low Leakage 6T (P110UL) bit cells to ensure high manufacturing yields

Five Power Modes: High Performance, Low Leakage, Standby, Retention, and Power Off modes provide flexibility for power optimization

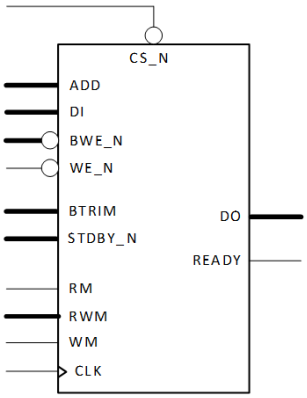
Speed Grades: Three options to adjust the speed/leakage balance and optimize for high speed or low power operation

Reverse Body Bias: Flexibility to make full use of FDSOI capabilities with optional pin selectable body bias settings

Memory Ready Output: Create a Pseudo-Dual Port memory utilizing the READY pin

High-Density Solutions: Abutment capability to enable multi-instance macros

Data Write-Through: Optionally prevent data out transitions during a write to reduce power



Technology	GF 22nm FDX
Voltage	0.8V (0.72V to 0.88V)
Temperature	-40°C to +125°C
Power	Mesh
# Metal Layers	4 (or 6 if 2 banks)
Speeds	Slow | Medium | Fast
BIST Mux	Internal
Modes	Functional, BIST, Scan, Sleep

Max Instance	640 Kilobits
Min Instance	256 Bits
Word Width	4 – 144
Banks	1 or 2
Word Depth	32 – 8192
Aspect Ratio	Column Fold: 4, 8 or 16
Redundancy (CMFOLD 8, 16)	Optional (4 or 8 repairs)
Write Enable	Optional Bit or Byte

EDA Views (Partial List)	
Verilog Model with UPF	
Liberty Files (NLDM, LVF, CCS)	
PDF and Text Datasheets	Redhawk APL
LEF 5.8	Verilog Test Bench
LVS SPICE Netlist	Bitmap File (x, y)
GDS	Power Grid (Voltus)
Tessent MBIST Control File	Common Power Format (CPF)

About Mobile Semiconductor:

Located in Seattle, Washington, Mobile Semiconductor develops SRAM, ROM, and Register File compilers optimized for applications requiring ultra-low power, low leakage, or ultra-high performance. Member of the GF® Partner Community.

http://www.mobile-semiconductor.com/