RF1P-ULL-GF22FDX-PLUS
Single Port Low Leakage
Register File Compiler

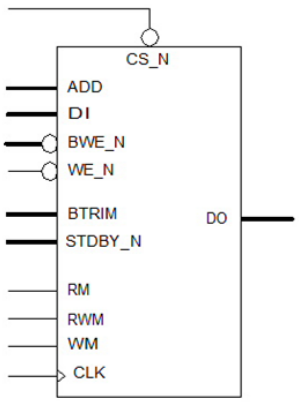
Ultra-Low Leakage: High V_T (HV_T) and low leakage HV_T ($LLHV_T$) devices used with source biasing to minimize standby currents while operating at low voltage

Bit Cell: Utilizes GlobalFoundries® Ultra-Low Leakage 6T (L110HD) bit cells to ensure high manufacturing yields

Four Power Modes: Active, Standby, Retention, and Power Off modes provide flexibility for power optimization

Speed Grades: Three options to adjust the speed/leakage balance and optimize for high speed or low power operation

Reverse Body Bias: Flexibility to make full use of FDSOI capabilities with pin selectable body bias settings



High-Density Solutions: Abutment capability to enable multi-instance macros

Data Write-Through: Optionally prevent data out transitions during the write to reduce power

Technology	GF 22nm FDX - PLUS
Voltage	.65V/0.8V typical
Temperature	-40°C to +125°C
Power	Mesh
# Metal Layers	4 with optional power connections in M5/C3
Speeds	Slow | Medium | Fast
BIST Mux	Optional

Max Instance	72 Kilobits
Min Instance	128 Bits
Word Width	4 – 72
Word Depth	64 – 2048
Aspect Ratio	Column Fold: 4 or 8
Write Enable	Optional Bit or Byte
Modes	Functional, BIST, Scan, Sleep

EDA Views (Partial List)	
Verilog Model with UPF	
Liberty Files (NLDM, LVF, CCS)	
PDF and Text Datasheets	Redhawk APL
LEF 5.8	Verilog Test Bench
LVS SPICE Netlist	Bitmap File (x, y)
GDS	Power Grid (Voltus)
Tessent MBIST Control File	Common Power Format (CPF)

About Mobile Semiconductor:

Located in Seattle, Washington, Mobile Semiconductor develops SRAM, ROM, and Register File compilers optimized for applications requiring ultra-low power, low leakage, or ultra-high performance. Member of the GF® Partner Community.

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